REMARKS

In the Office Action, the Examiner noted that claims 1-22 are pending in the application and that claims 1-22 are rejected. By this response claims 1, 3-6, 11, 16 and 20 are amended to more clearly define the invention of the Applicants and to correct for informalities pointed out by the Examiner and not in response to prior art. All other claims are un-amended by this response.

In view of the above amendments and the following discussion, the Applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, the Applicants believe that all of these claims are now in allowable form.

Objections

A. Claims 3 and 4

The Examiner objected to the Applicants' claims 3 and 4 stating that in line 1 of claims 3 and 4, "said apparatus" lacks clear antecedent basis.

In response, the Applicants have herein amended claims 3 and 4 to specifically recite "Apparatus of claim 1, wherein...", thus making clear claims 3 and 4. Having done so, the Applicants respectfully submit that the basis for the Examiner's objection to the Applicants' claims 3 and 4 has been removed. As such, the Applicants respectfully request that the Examiner's objections to the Applicants' claims 3 and 4 be withdrawn.

Rejections

A. 35 U.S.C. § 103

The Examiner rejected claims 1-5 under 35 U.S.C. §103(a) as being unpatentable over Lindberg (U.S. Patent No. 6,366,579) In view of Sharony et al (U.S. Patent No. 5,495,356, hereinafter "Sharony"). The rejection is respectfully traversed.

The Examiner alleges that regarding claims 1-5 Lindberg discloses in Figs. 11-12 a space/time switching unit wherein the data words in the received

time slots are disassembled to bit level such that each data word is divided into a number of bits, BIT0 to BIT7. The Examiner further alleges that each bit is then distributed to a respective row of speech stores SS of that row. The Examiner further alleges that the multiplexers, 8/1 MUXs, controlled by the associated control stores, CS, are operative to output selected bits from the speech stores. The Examiner concedes however, that Lindberg does not disclose an apparatus for conveying said selected bit pack to any output data position within a combination of output data rails and time slots. As such, the Examiner cites Sharony for disclosing a system in which an input and/or N inputs are connected to a passive broadcast medium that broadcasts an input and/or all the inputs to each one or all N outputs. Thus the Examiner alleges that it would have been obvious to one having ordinary skill in the art to include the apparatus of Sharony in the system of Lindberg.

The Applicants respectfully submit that the teachings of Lindberg or Sharony, alone or in any allowable combination do not teach, suggest or make obvious the invention of the Applicants, at least with respect to claims 1-5. More specifically, the Applicants' amended claim 1 specifically recites:

> "Apparatus for switching data from any of a plurality of inputs to any of a plurality of outputs, comprising:
> at least one apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots **and for storing said received bit packs in matrix form including a storage position for each rail and time slot combination,**
> at least one apparatus for selecting any of the input bit packs from any of the rails in any of the time slots of said matrix, and
> at least one apparatus for conveying said selected bit pack to any output data position within a combination of output data rails and time slots." (emphasis added).

In support of at least claim 1, the Applicants, in the Specification specifically recite:

> "In this illustrative embodiment, the first bits of 4 input channels, c1b1 through c4b1 are switched to the first bits of 4 output channels, c5b1 through c8b1. A 4 to 2 multiplexer 402, multiplexes bit-pack, first bits routed to the switching core 400 from various disassemblers, to 2 to 1

multiplexers 404, 406, 408, and 410. In this illustrative embodiment, during the first time slot, the multiplexer 402 selects bits c1b1 and c2b1 and routes those bits to 2 to 1 multiplexers 404-410. During the second time slot, the multiplexer 402 selects bits c3b1 and c4b1 and routes them to the 2 to 1 multiplexers 404-410. In this manner, each of the 2 to 1 multiplexers 404-410 may select any input, c1b1 through c4b1 to latch into a storage area 412-418, respectively. The storage areas 412-418 are often depicted, and will be hereinafter, as a switch matrix that may correspond to a combination of time slots and physical connection paths referred to as ralls." (See Specification page 10, lines 1-11).

And

"The input data bits of the illustrative embodiment can be represented by a matrix such as shown in figure 6, in which each row represents a rail and each column represents a time slot. Each incoming STS-1 signal's data bit may be placed by a rail number and a slot number. Such a matrix will be referred to hereinafter as an input bit map. Similarly, the switches output may be represented by an output bit map in which each outgoing STS-1 channel is identified by an outgoing rail number and time slot number. A physical embodiment for the input and output bit maps may be realized by employing a selection block, 701, as in Fig. 7, for each of the seven hundred and sixty eight input or output data bits of the illustrative embodiment." (See Specification, page 11, lines 20-27).

And

"Figure 7 provides a conceptual block diagram of an illustrative embodiment of such a space/time implementation 700, which will be referred to hereinafter as an expander space/time switch. Such a configuration employs a selection block 701 for each of the seven hundred and sixty eight locations in the switch core's output bit map." (See Specification, page 12, lines 25-29).

It is evident from at least claim 1 and the portions of the Applicants' Specification presented above, that the Applicants' invention is directed at least in part to an apparatus for switching data including at least an apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots **and for storing the received bit packs in matrix form including a storage position for each rail and time slot combination.** Furthermore, in various embodiments of the Applicants' invention, the apparatus of the Applicants' invention includes a selection block for each storage position in the matrix. As such, the apparatus of the Applicants' invention as taught in the Applicants' Specification and claimed by at least the Applicants' claim 1 is

capable of switching data from any of a plurality of inputs to any of a plurality of outputs.

The Examiner concedes that Lindberg fails to teach, suggest or make obvious an apparatus for conveying said selected bit pack to any output data position within a combination of output data rails and time slots. The Applicants agree. However, the Applicants submit that Lindberg further fails to teach, suggest or make obvious, at least an apparatus (e.g., a switching core) for receiving a plurality of input bit packs organized in a combination of input data rails and time slots **and for storing the received bit packs in matrix form including a storage position for each rail and time slot combination** as taught in the Applicants' Specification and claimed by at least the Applicants' claim 1. More specifically, in contrast to the invention of the Applicants, at least with respect to claims 1-5, Lindberg, as pointed out by the Examiner, specifically recites:

> "The subrate switch SRS comprises a matrix of speech stores SS, and associated multiplexors and control stores. However, the speech stores SS in the subrate switch SRS are prepared to store bits instead of entire words in the storage positions. The subrate switch SRS is further equipped with an input terminal IN and an output terminal OUT. The time slots that are provided to a predetermined input terminal of the TS-module XMB is also distributed to the input terminal IN of the subrate switch SRS such that the subrate switch SRS is continuously supplied with time slots. In the subrate switch SRS, the data words in the received time slots are disassembled to bit level such that each data word is divided into a number of bits BIT0 to BIT7. Each bit is then distributed to a respective row of speech stores in the subrate switch SRS, and stored in all speech stores SS of that row. The multiplexors 8/1 MUXs controlled by the associated control stores CS are operative to output selected bits from the speech stores. The selected output bits of the multiplexors 8/1 MUX in the subrate switch SRS are combined in a bits-to-word converter into an entire word which is sent to the TS-module XMB." (See Lindberg, col. 18, lines 41-48).

In the invention of Lindberg, at least with respect to the embodiment of FIG. 11, a received data word is disassembled to bit level such that each data word is divided into a number of bits BIT0 to BIT 7. Each of the bits is then distributed to

and stored in all of the speech stores of a respective row. The multiplexors 8/1 MUXs then output selected bits from the speech stores in column format. More specifically, in Lindberg, each bit is stored in all of the speech stores of a respective row. That is, BIT0 of a data word is stored in all of the speech stors one of row; BIT1 is stored in all of the speech stores of row two, BIT3 is stored in all of the speech stores in row three...and so on. Multiplexors in Lindberg then select a bit from column one, a bit from column two...for all of the columns.

In contrast, in the invention of the Applicants, the teachings of Lindberg alone do not teach, suggest or make obvious the invention of the Applicants' regarding at least an apparatus (e.g., a switching core) for switching data from any of a plurality of inputs to any of a plurality of outputs including "at least one apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots **and for storing said received bit packs in matrix form including a storage position for each rail and time slot combination"** as taught in the Applicants' Specification and claimed in at least the Applicants' claim 1.

For at least the reasons stated above and as conceded by the Examiner, the Applicants respectfully submit that the teachings of Lindberg, alone, fail to make obvious the invention of the Applicants, at least with respect to claim 1. Furthermore, the Applicants respectfully submit that the Sharony reference alone also fails to teach, suggest or make obvious the invention of the Applicants, at least with respect to claims 1-5. The Applicants respectfully submit that there is absolutely no teaching, suggestion or disclosure in Sharony for at least an apparatus (e.g., a switching core) for switching data from any of a plurality of inputs to any of a plurality of outputs including "at least one apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots **and for storing said received bit packs in matrix form including a storage position for each rail and time slot combination"** as taught in the Applicants' Specification and claimed in at least the Applicants' claim 1.

In contrast, Sharony teaches a switching network that utilizes at least three degrees of freedom, time, wavelength and space. In one embodiment of Sharony, each space channel between an input and an output is assigned a time slot and wavelength coordinate characteristic of the output and the input transmitter and output receiver are tuned to the appropriate time and wavelength coordinates and selective switching is used to complete the space channel between the input and output. In another embodiment of Sharony, each input channel is assigned a set of space, time slot and wavelength coordinates and an input signal is broadcast to all of the outputs which selectively makes connection to those inputs with an appropriate set of coordinates. (See Sharony, Abstract). In contrast to the Applicants' invention, however, Sharony specifically teaches:

> "The STSW has two stages, the first stage shown in FIG. 3 is composed basically of n mxm star couplers 31, and the second stage shown is composed of m nxln Wavelength-Time Selective Switches 32 (WTSSs). The two stages are connected to each other by mn optical links 33, that may be optical fibers. To each one of the n star couplers 31, m optical transmitters 34 are connected, each fixed with a different wavelength (e.g., .lambda..sub.0, .lambda..sub.1, ...lambda..sub.m-1). Each optical transmitter 34 is driven by an electrical signal composed of l inputs multiplexed in time (e.g., t.sub.0,t.sub.1, . . . t.sub.l-1) by a time division multiplexer 35. Thus, each input channel space is uniquely identified by a triplet indicating the fixed sub-channels it uses in each of the three dimensions, i.e., (s.sub.i, .lambda..sub.j, t.sub.p). Each WTSS 32 has ln outputs and it receives the entire information from all the N inputs." (See Sharony, col. 5, lines 46-60). (emphasis added).

In the invention of Sharony, each of the WTSS receives the entire information from all the N inputs. However, the invention of Sharony does not teach, suggest or make obvious an apparatus (e.g., a switching core) for switching data from any of a plurality of inputs to any of a plurality of outputs including "at least one apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots **and for storing said received bit packs in matrix form including a storage position for each rail and time slot combination"** as taught in the Applicants' Specification and claimed in at least the Applicants' claim 1.

Furthermore, the Applicants submit that there is absolutely no suggestion or motivation in any of the references to combine the teachings of Lindberg and Sharony as suggested by the Examiner.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983).

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

The Applicants further submit that even if a suggestion to combine the references as suggested by the Examiner did exist (which the Applicants submit that no such suggestion exists), the Examiner's attention is directed to the fact that the alleged references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious the Applicants' invention, at least with regard to the Applicants' independent claim 1. The substantial gap between the teachings of Lindberg and the invention of the Applicants is not bridged by the teachings of Sharony. More specifically, the combination of the teachings of Lindberg and Sharony fail to teach, suggest or make obvious at least an apparatus (e.g., a switching core) for switching data from any of a plurality of inputs to any of a plurality of outputs including "at least one apparatus for receiving a plurality of input bit packs organized in a combination of input data

rails and time slots **and for storing said received bit packs in matrix form including a storage position for each rail and time slot combination"** as taught in the Applicants' Specification and claimed in at least the Applicants' claim 1.

Therefore, the Applicants respectfully submit that claim 1, as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Likewise, independent claim 5 recites similar relevant features as recited in claim 1. As such, and for at least the reasons stated herein with respect to claim 1, the Applicants further submit that Lindberg and Sharony, alone or in any allowable combination, do not teach, suggest or make obvious independent claim 5. As such, the Applicants respectfully submit that claim 5 as it now stands, also fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Furthermore, dependent claims 2-4 depend directly from independent claim 1 and recite additional limitations therefore. As such and for at least the reasons set forth above, the Applicants submit that none of these claims are obvious with respect to the teachings of Lindberg and Sharony, alone or in any allowable combination. Therefore, the Applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

The Applicants reserve the right to establish the patentability of each of the claims individually in subsequent prosecution.

B. 35 U.S.C. § 103

The Examiner has rejected claims 6-22 under 35 U.S.C. § 103 as being unpatentable over Sharony in view of Lindberg. The rejection is respectfully traversed.

The Examiner alleges that regarding claims 6 -22, Sharony discloses in Fig. 3, a multidimensional switching network for broadcasting any of the input data to a plurality of output channels. However, the Examiner correctly concedes

that Sharony does not disclose wherein the data is formatted as data blocks containing a fixed number of bits of data, each data block comprising "O" bit packs containing a number of bits "P", where O and P are integers. As such, the Examiner cites Lindberg for teaching such limitations. The Applicants respectfully disagree.

For at least the reasons recited above with respect to the Examiner's rejection of claims 1-5 of the Applicants' invention, the Applicants further submit that the teachings of Sharony and Lindberg, alone or in any allowable combination, fail to teach, suggest or make obvious the invention of the Applicants at least with respect to claims 6-22. More specifically, the Applicants' independent claims 6, 11, 16 and 20 recite similar relevant features as recited in the Applicants' independent claim 1. As such, at least because Lindberg and Sharony, alone or in any allowable combination, fail to teach, suggest or make obvious the Applicants' claim 1 with regards to at least an apparatus (e.g., a switching core) for switching data from any of a plurality of inputs to any of a plurality of outputs including "at least one apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots **and for storing said received bit packs in matrix form including a storage position for each rail and time slot combination**" as taught in the Applicants' Specification and claimed in at least the Applicants' claim 1, the Applicants further submit that the teachings of Lindberg and Sharony, alone or in any allowable combination, also fail to teach, suggest or make obvious the Applicants' independent claims 6, 11, 16 and 20, which recite similar relevant features as the Applicants' independent claim 1.

Therefore and for at least the reasons stated above, the Applicants respectfully submit that independent claims 6, 11, 16 and 20 as they now stand, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Furthermore, dependent claims 7-10, 12-15, 17-19 and 21-22 depend either directly or indirectly from independent claims 6, 11, 16 and 20 and recite further limitations therefore. As such and for at least the reasons set forth above,

the Applicants respectfully submit that none of these claims are obvious with respect to the teachings of Lindberg and Sharony, alone or in any allowable combination. Therefore, the Applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

The Applicants reserve the right to establish the patentability of each of the claims independently in subsequent prosecution.

Conclusion

Thus, the Applicants submit that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. § 103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Jorge Tony Villabon, Esq. at (732) 383-1396 or Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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